FACULTY PROFILE

Name : **SRIVIDYABARATHI A**

Date of Birth and Age : **19.11.1994** and **30 years**

Academic Qualification and Performance :

Degree/ Diploma	Programme /Specialization	% of Marks/CGPA	Class	Month & Year of passing	University
B.E	E.C.E	8.411	First Class with Distinction	May 2015	ANNA UNIVERSITY
M.E	Communication Engineering	8.55	First Class with Distinction	May 2018	ANNA UNIVERSITY
Ph.D	Electronics and Communication Engineering	-	-	Pursuing	ANNA UNIVERSITY

Employment Details:

Name of the College/Industry	Position	Experience (From - To)
GOVERNMENT COLLEGE OF TECHNOLOGY	ASSISTANT PROFESSOR(Contractual)	20.06.2018 -till date

Total Experience (In Academics) : 7 Years 4 months

Publication In International/National Journals/Conferences: Journal:

1. **A.Srividyabarathi,** "High Performance and Efficient Reversible Multiply Accumulate Unit" International Journal of Science and Innovative Engineering & Technology (IJSIET), http://ijsiet.org/content.htm, Volume 2 May issue 2018, ISBN No. 978-81-923607-3-7.
2. **M, Vishva Sakthi, Sathiya Prakash B L, and Srividyabarathi A.** "Low Power and Delay Efficient 4x4 Array Multiplier Using 20T Hybrid Adder in 90nm Technology." Journal of Electronics and Informatics 6, no. 2 (2024): 140-156. https://doi.org/10.36548/jei.2024.2.006

Conferences:

National:

1. M, Vishva Sakthi, Sathiya Prakash B L, and Srividyabarathi A. "Low Power and Delay Efficient 4x4 Array Multiplier Using 20T Hybrid Adder in 90nm Technology." a paper presented in National Conference on Electrical and Instrumentation Systems(NCEIS'24) held at Government College of Technology, Coimbatore during June 07, 2024.
2. Abishekkumar A, Prathipa L, Dr.Deepa P, Srividyabarathi A, "High Speed and Low Power Full Adder using 16T Hybrid Design in 90nm Technology " a paper presented in National Conference on Advanced Computing and Communication Systems(NCACCS'25) held at Government College of Technology, Coimbatore during March 27, 2025.

Participation in FDP/STC:

1. Completed the 8 weeks FDP course “System Design through Verilog” on NPTEL form July to September 2022.
2. Participated in Six Days Short Term Course on “Analog ICs and Semiconductor Advancements in VLSI” organized by Department of ECE,NIT-DELHI from 10th to 15th February 2025.
3. Participated and Completed 40hours Online Training Program cum FDP on “ Foundations of VLSI Design Verification” organized by Electronics and ICT Academics MNIT Jaipur, IITDM Jabalpur, IIT Roorkee & NIT Patna and supported by MeitY from 23rd June to 5th July 2025.

Participation in Conferences/ Seminars/ Workshop:

1. Participated in NIELIT sponsored 4 weeks online Lab Workshop on “FPGA Architecture and Programming using Verilog HDL” jointly organized by Arm Education and NIELIT Calicut during 28th December 2022 to 25th January 2023.
2. Participated in One day hands on training on “Full Custom Design Flow using Cadence EDA Tool” on 10th February 2023.
3. Participated in One-day workshop on “PYNQZ2 FPGA Evaluation Kit” organized and conducted by Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore on 20th April 2023.
4. Participated in 5 Days workshop on “VLSI to System Design: Silicon to End Application Approach” organized by AICTE, Arm Education and STMicroelectronics from 31st July to 4th August 2023
5. Participated in Two Days workshop on “Analog Physical Design using Cadence EDA Tool” conducted by Department of ECE,SREC in association with ISTE student Chapter and Entuple Technologies Pvt. Ltd., Bengaluru on 13th and 14th October 2023.
6. Participated in Three Day Workshop on “Cadence Analog, Digital and Mixed Signal Flow” organized and conducted by Department of Electronics and Communication Engineering, Government College of technology, Coimbatore from 26th to 28th February 2024.
7. Participated in 3 Days Workshop on “Cadence Semi- Custom and Full Custom IC Design” organized and conducted by Department of Electronics and Communication Engineering, Government College of technology, Coimbatore from 9th to 11th September 2024.
8. Participated in Three days workshop on “Synopsys Digital and Analog VLSI Design Flow” organized by Department of ECE in association with VLSI Minds and C2S from 29th to 31st October 2025.

I hereby declare that all the above information furnished is true to the best of my knowledge and belief.

(A.SRIVIDYABARATHI)

Signature